FAULT-TOLERANT INVERTER FOR HIGH-SPEED LOW-INDUCTANCE BLDC DRIVES IN AEROSPACE APPLICATIONS

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ABSTRACT: Due to the simplicity and high reliability, brushless dc (BLDC) motors are widely used in space application. High reliability levels are the vital aspect for ensuring the long term stable operation of the BLDC motor system which is used in aerospace applications. The fault tolerant control of BLDC motor is of great importance for its continuous operating capacity even under the faulty situation. This paper proposes a fault tolerant topology composed of an additional phase leg and a fault protective circuit for the high-speed low-inductance BLDC motor. Based on the analysis of the overcurrent and overvoltage phenomenon after the switch faults, a novel fault isolation and system reconfiguration method is presented. The method can achieve safe isolation and reconfiguration to avoid the secondary fault caused by direct switch of the redundant switch and the faulty switch after the fault diagnosis process. Both simulation and experimental results confirm the feasibility and effectiveness of the proposed method.

INDEX TERMS: Brushless dc (BLDC) motor rush less dc (BLDC), buck converter, buck converter, system reconfiguration fault tolerant topology

I. INTRODUCTION

Magnetically suspended control moment gyroscope (MSCMG) has attracted a great deal of attention for its significant application in attitude control of spacecraft. It has the encouraging advantages of high-precision, large-moment and long-life owing to the zero friction and enhanced damping of a high-speed rotor. The reliability of the machine drives is one of the most important factors to guarantee the safe, continuous and high performance operation even under some accidents or faults. The work mentioned that power semiconductor device faults account for about 35% of all motor systems faults, and up to 40% of the three-phase inverter failures occurring due to the power switches. Since the capability of human intervention is limited in space application, the fault isolation and system reconfiguration measure based on reliable fault diagnosis methods is an effective means to ensure the continuous operating capacity after the inverter faults. As an important part of MSCMG for space application in vacuum, the high-speed rotor drive system demands high operating speed and low power loss.

Thus the brushless dc (BLDC) motors with an ironless and spotless stator are always used. Generally, phase pulse width modulation (PWM) control method is extensively applied in high-power/low-power BLDC motor drives with a three phase full bridge inverting circuit. Unfortunately, it would induce serious current and torque ripples for the ironless stator motor which tends to have very low inductance. Moreover, the high-frequency and large-range current ripple will inevitably increase the copper and rotor iron losses. In order to achieve low power consumption, a PWM controlled buck type DC-DC power converter in front of the three phase bridge inverter is employed for the low inductance BLDC motor drive of MSCMG.

However, the introduction of the buck type DC-DC power converter changes the characteristics of three full bridge inverting
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The system reconfiguration methods with the redundant hardware topology design which have the advantages of high reliability have attracted many researchers in the recent decades. The research proposes an improved induction motor drive topology with redundant triacs and fuses. The control strategy introduced in this paper allows continuous, disturbance free operation of the drive after inverter or motor phase faults. Correa et al. present a fault tolerant topology with a redundant phase leg connected to the neutral point permitting the fault-tolerant operation of a three-phase induction motor drive system.

The research proposes a remedial strategy against inverter failures based on the same topology to achieve smooth torque for PMSM drives. It should be noted that the proposed fault tolerant topologies may unavoidably increase the system currents and power loss and decrease the maximum motor torque in their post fault operations. The additional leg topology with a redundant phase leg connected to the three phase windings is adopted.

This topology can provide rated post fault power without the overrating of power devices. And the output torque is similar to that of the Perrault operation without excessive torque ripple. Back-to-back-connected thyristors are applied in place of electromechanical relays used to achieve fast post fault isolation and reconfiguration. However, for low power applications, the on-state resistance of the thyristors may increase the system power loss. The integrated fault compensation strategies for two different types of configurations of induction motor drive systems are presented. The proposed strategies allow for continuous free operation of the drive after open-circuit or short-circuit failure occurring in the converter power devices. An improved fault-tolerant control scheme for PWM inverter-fed induction motor based electric vehicles is proposed, which is based on 4-wire and 4-leg PWM inverter topologies after IGBT open-circuit faults.

The software FTC methods can guarantee the safe, continuous operation after some accidents or faults by the FTC algorithm design without hardware redundancy. In order to suppress the low-frequency pulsating torques for a vector-controlled induction motor drive in inverter fault conditions, a general purpose search algorithm is proposed, which fabricates the desired harmonic voltage magnitudes and phase angles. Nevertheless, it has some limitations when used in practice because that this method is only effective for the neutral connection of the machine. A fault-tolerant torque control method for switch faults is presented to optimally reshape the phase currents of the remaining phases with the purpose of minimizing power loss of the post fault operation. However, the software calculation algorithm is complicated. Also, the post fault operation scheme will unavoidably increase the system currents and power loss. It should be noted that the fault tolerant topology and reconfiguration methods all deal with the switch fault in traditional three-phase inverter.

A proper fault tolerant topology including a redundant buck converter and a redundant three-phase bridge should be presented. Meanwhile, according to the analysis, the switch fault features in traditional three-phase inverter and the inverter with a buck converter and a three-phase full bridge are different. The traditional post fault switch
scheme is not suitable for the novel fault tolerant topology. It is meaningful to propose a system reconfiguration scheme after the switch faults for the high-speed low-inductance BLDC motor to ensure high reliability of the high-speed motor drive system in the MSCMG. This system proposes a fault tolerant topology and a system reconfiguration scheme based on the fault diagnosis method for the high-speed low-inductance BLDC motor in space application. The proposed fault tolerant topology is composed of an additional phase leg and a fault protective circuit. With the analysis of the over current and overvoltage phenomenon after the switch faults, a fault isolation and system reconfiguration method is proposed.

II. Proposed Method: The overall fault-tolerant BLDC motor driver configuration is shown in Fig. 1, which includes a redundant three-phase full bridge, a redundant buck converter and a fault protective circuit. Similarly, the buck converter is used to adjust the current of the windings, and the current control type is applied to the buck converter. The redundant switch T10 is the hardware backup of the buck converter switch T7. The switches Q1 and Q2 are used to isolate the faulty switch and connect the redundant switch after the switch fault in the buck converter. The fourth leg composed of switches T8 and T9 is used as a hardware backup of the three phase full bridge. Six triacs Sa, Sb, Sc, Sra, Srb, Src are used to compose the fault switching circuit of three-phase full bridge.

![Fig.1. Proposed fault-tolerant topology for inverter of high-speed BLDC motors.](image-url)
**DESCRIPTION**

Buck Boost Converter having 4 Switches (Mosfets), which is used to either buck or boost the input DC Voltage based on User's Input.

If the Input DC Voltage is too high then the Circuit automatically bucks the input voltage and provides to load. If the input DC voltage is low then it boosts the Load.

Fault Protector is used to protect the entire circuit.

The heart of the Circuit is designed based on Mosfets (T1, T3, T5, T4, T6 and T2) [Refer.Fig1], if any Mosfet mentioned above is in fault, the load will getting affected, so the fault tolerant circuit immediately off the entire 3-Phase Circuit, so that we can prevent the load from high voltage level or some other faults.

Fault Switching Circuits, which uses 6 Triacs, to identify which Mosfet is affected in the Heart of the Circuit.

Hardware Backup Drivers, in circuit they mentioned 2 additional Mosfets (T8 and T9) to indicate the Hardware Backups.

3-Phase Bridge, is used to convert the single phase to 3-phase.

The fault protective circuit composed of a power resistance R1 and a MOSFET T11 is used to isolate the overvoltage phenomenon caused by the switch open-circuit or short-circuit faults in the three-phase full bridge or the buck converter.

The initial inverter topology and post fault inverter topologies after switch fault in buck converter or three-phase full bridge are illustrated in Fig. 2. Fig. 2 (d) shows the post fault inverter topology after succession switch faults in both buck converter and three-phase full bridge.
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Fig. 2. The initial and post fault topology of the proposed fault-tolerant inverter. (a) Fault-free topology, (b) Post fault topology of fault type F1 or F2, (c) Post fault topology of fault type F3 or F4, (d) Post fault topology of fault type F1 or F2 and fault type F3 or F4.

Neglecting the very low stator inductance of the motor, the voltage equations of fault-free inverter topology S0 derived from the state-space averaging method are written as

\[
\begin{align*}
    u_o &= u_{in} - \Delta u_{dio} (1-d_1) - L_c d_i \frac{di}{dt} - 2R_i d_i \\
    C_o \frac{di}{dt} &= i_L - i \\
    u_0 &= 2R_i i + e_L + \Delta u_{uv} 
\end{align*}
\]  

(1)

where \( u_{in} \) and \( u_0 \) are the input and output voltages of buck converter, \( L_f \) and \( C_0 \) are the inductance and capacitor of buck converter, \( i_L \) is the inductance current in buck converter, \( i \) is the dc-link current of the motor, \( \Delta u_{dio} \) is the forward voltage of the diode D0 and D1, \( R_p = R + R_m + R_t \), \( R \) is the stator resistance, \( R_m \) is the MOSFET on-state resistance, \( R_t \) is the triac on-state resistance, \( e_L \) is the line-to-line back EMF voltage satisfying \( e_L = e_{up} - e_{elow} \), \( e_{up} \) and \( e_{elow} \) are back EMF voltages of the upper and lower side conducting phases, \( d_1 \) is the duty cycle of the switch T7.

Depending on the fault-tolerant drive system, the first three topologies all have certain fault-tolerant capacity. The faults should be detected and identified in order to realize the post-fault strategies are classified as

1) Open-circuit damage of switch in redundant buck converter (F1);
2) Short-circuit damage of switch in redundant buck converter (F2);
3) Open-circuit damage of single switch in redundant three phase bridge (F3);
4) Short-circuit damage of single switch in redundant three phase bridge (F4).

Taking the switch fault of T1 in the three-phase full bridge or switch T7 fault for example, the topology modes of the proposed fault-tolerant inverter topology are classified as

1) Fault-free inverter topology (S0) shown in Fig. 2 (a);
2) Post fault inverter topology of fault type F1 or F2 (S1) shown in Fig. 2 (b);
3) Post fault inverter topology of fault type F3 or F4 (S2) shown in Fig. 2 (c);
4) Post fault inverter topology of switch fault in buck converter (fault type F1 or F2) and single switch fault in the
Simulation Results:
CONCLUSION

In this system, a fault tolerant topology and a system reconfiguration scheme for the high-speed low-inductance BLDC motor used in space application is proposed. The method can achieve safe post fault isolation and reconfiguration to avoid the secondary fault caused by direct switch of the redundant switch and the faulty switch after the fault diagnosis process. The system reconfiguration can be implemented rapidly and effectively after the open-circuit or short-circuit switch fault by the proposed method. Simulated and experimental results verify the validity of the proposed fault diagnosis method.

REFERENCES


