DESIGN AND IMPLEMENTATION OF RNS REVERSE CONVERTER USING PARALLEL PREFIX ADDERS

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ABSTRACT - In this paper, the implementation of residue number system reverse converters based on hybrid parallel prefix adders is analyzed. The parallel prefix adder provides high speed and reduced delay arithmetic operations but it is not widely used since it suffers from high power consumption. Hence, a hybrid parallel prefix adder component is presented to perform fast modulo addition in Residue Number System reverse conversion. The proposed components are not only results in fast arithmetic operation and it also highly reduced the hardware complexity since it requires fewer amount of logic elements. In this work, the proposed components are implemented in Xilinx and different moduli sets reverse converter designs and the performances are compared for different values of n.

KEYWORDS: Digital Arithmetic, Parallel-prefix adder, Residue number system (RNS), Reverse converter.

I. INTRODUCTION

The Residue Number System plays a significant role in the battery based and portable devices because of its low power features and its competitive delay. The Residue number framework turn around converter is planned with parallel prefix expansion by utilizing new segments approach for higher speed operation. The RNS comprises of two principle parts forward and the turnaround converter that are coordinated with the current computerized system[5]. The forward converter plays out the operation of changing over the double number to the modulo number while the turnaround converter plays out the operation of switch changing over the modulo number to the binary number which is the hard and time consuming process compared with the forward converter[3]. The fundamental RNS concepts such as 1)RNS definition with properties and their applications,2)consideration of modulo set selection,3)design of forward converter,4)modulo arithmetic units,5)design of reverse converter are discussed[2].

The voltage over scaling (VOS) technique is applied to the residue number system to achieve high energy efficiency [7]. The VOS technique introduces soft errors which degrades the performance of the system. To overcome these soft errors a new technique is implemented called joint RNS-RPR which is the combination of RNS and the reduced precision redundancy. This method provides the advantage of satisfying the basic properties of RNS includes shorter critical path, reduced complexity and low power. New architectures are presented for the moduli set (2n-1,2n, 2n+1) for the conversion from the residue to the binary equivalents. Here the speed and the cost are major concern[9,10].

Distributed arithmetic principles are used to perform the inner product computation[8]. The input data which are in the residue domain which are encoded using the Thermometer code format and the outputs are encoded using the one hot code format. Compared to the conventional method which used Binary code format, the proposed system which achieves higher operating speed. The residue number system which provides carry free addition and fully arithmetic operation, for several applications such as digital signal processing and cryptography.

In this brief, we present a comprehensive method which uses the parallel prefix adder in selected position, thereby using the shift operation on one bit left to design a multiplier on the same design module to achieve a fast reverse converter design. The utilization on parallel prefix structure in the plan prompts to higher speed in operation in the mean time it expands the range and power utilization. With a specific end goal to remunerate the tradeoff between the speed, region and power utilization, a novel particular cross breed parallel prefix based
snake segments are utilized to plan the invert converter.

II. LITERATURE REVIEW

To design a converter that may be either forward or reverse contain specific procedures. The arithmetical units are the prime concern in the residue based digital systems. To make efficient design of reverse converter we have to follow the procedures. The reverse converter design efficiency will depend on the two factors are selection algorithm, selection of moduli set. The proper selection these two factors will yields the efficient design of reverse converter since its design has complex and non modular architecture. Still the selection of hardwares resources used in the converters will affect the performance of the reverse converter. The modulo adders are the conventional resources that are using in reverse converters. The modulo ripple carry adder will have simple structure yet affects from longer propagation delay whenever number of bits are growing for the inputs. The modulo parallel prefix adder will compute carries initially based on set of prefix networks even though having high speed lagging in area due to long prefix networks which causes area. The converters that are designed based on this adders will also be inefficient as like as them. To avoid all these drawbacks we are designing anew converters that is also based on the prefix adders with slight changes to them which makes area efficient without affecting the speed performance. The proposed adders are efficient hence the new converters will also have sufficient trade off between the area and speed. The new adder architectures are presented in subsequent chapters. Parallel-prefix adders with its fast component have been utilized as a part of the RNS measured number juggling channels. This execution pick up is because of parallel convey calculation structures, which depends on various calculations. Each of these structures has unmistakable attributes, for example, Sklansky (SK), and Kogge–Stone (KS) as they have the most extreme and least fan-out, individually, both giving insignificant rationale profundity. Least fan-out comes to the detriment of more circuit range [18]. In this manner, equipment parts determination ought to be embraced deliberately.

Fig.1: PPX structure.

III. PROPOSED NOVEL COMPONENTS

The First proposed reverse converter with large dynamic range is Ripple carry adder based reverse converter. It suffers from the delay whenever there is increase in the number of residues that should perform addition which affects the speed of the design[1]. To improve its speed high speed parallel prefix adders will be employed, they consist more prefix networks to compute the carry which makes less efficient area. The number of prefix networks will increase logarithmically when the number of bits that are to be added are growing. We already discussed that reverse converter algorithm will composed of certain number of addition. Each and every adder has to be carefully designed. The addition that was coming at the final stage in the algorithm will plays vital role on performance of converter. That parameters will impact on whole algorithm. The adder used at the final stage of conversion will have usually two inputs. One of input contain 4n+1 bits. The second will contain 2n+1 bits. To make the second operand as 4n+1 bits we will add constant 2n+1 bits to the second operand which accomplishes the addition. Such that we don’t need any extra prefix network to the addition MSB 2n+1 bits in the two operands. At this step we are reducing the size of prefix networks to half such as 4n+1 adder will may contain only 2n+1 prefix networks. The remaining biot addition will be accomplished as per lemma shown below Lemma: According to this the between two of the operands that are applying to final stage adder will have 2n+1 constant bits and they are equal to 1. In the final stage of algorithm we actually perform subtraction between the operands that are applying to it. To perform this we actually need a subtractor. We are using an adder that to perform
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IV. NEW PARALLEL-PREFIX BASED COMPONENTS

The HMPE Structure comprises of two sections: Regular prefix viper and the Modified Excess One unit. The initial two operands are included utilizing the parallel prefix viper and the outcome is restrictively augmented in view of the control flag produced by the prefix structure to guarantee the single zero representation. The below figure shows HMPE Structure.

V. RESULTS

VI. CONCLUSION

The reverse converter which actually used in conversion of numbers from residues to binary values. This is actually used in residue based arithmetic devices where residue number system has vital role. Since the residue number system will increase the speed of processing due to carry free addition, borrow free subtraction and parallel
pipelining. These are the advantages that make residue number system effective. The proposed converter will be designed to reduce the delay caused by RCA and large area caused by parallel prefix adder due to more number of stages. The HRPX and HMPE are the modules that are designed to achieve less are and speed trade off. The HRPX and HMPE initially designed and verified then remaining modules are designed all modules are Connected to -gether to perform reverse conversion. The designing is achieved through the Verilog HDL, then they are synthesized and simulated in Xilinx 13.2 i. The results are proving that it s having good tradeoff between area and speed.

REFERENCES


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