LOW POWER AND HIGH FAULT COVERING TPG BIST TECHNIQUE USING LP-LFSR

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ABSTRACT: - This paper presents a novel test pattern generator which is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. A new method for test pattern generation (TPG) in a built-in self-test (BIST) environment is proposed here. The TPG uses the characteristic information of the circuit to generate the test vectors internally. The characteristic information of the circuit is extracted using known spectral methods. The objective of the BIST is to reduce power dissipation without affecting the fault coverage. The proposed test pattern generator reduces the switching activity among the test patterns at the most. In this approach, the single input change patterns generated by a counter and a gray code generator are Exclusive–ORed with the seed generated by the low power linear feedback shift register [LP-LFSR]. The proposed scheme is evaluated by using, a synchronous pipelined 4x4 and 8x8 Braun array multipliers. The System-On-Chip (SOC) approach is adopted for implementation on Xilinx Field Programmable Gate Arrays (FPGAs). From the implementation results, it is verified that the testing power for the proposed method is reduced by a significant percentage.

KEYWORDS - FPGA, BIST, LP-LFSR, Switching activity

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits [1]. The ability to design, fabricate and test Application Specific Integrated Circuits (ASICs) as well as FPGAs with gate count of the order of a few tens of millions has led to the development of complex embedded SOC. Hardware components in a SOC may include one or more processors, memories and dedicated components for accelerating critical tasks and interfaces to various peripherals. One of the approaches for SOC design is the platform based approach. Power dissipation is a challenging problem for today’s System-on-Chips (SOCs) design and test. In general, the power dissipation of a system in test mode is more than in normal mode [2]. Four reasons are blamed for power increase during test [3].

Real time imaging processes require intensive scientific computations for Digital Signal Processing (DSP). Fast and efficient parallel multipliers are required for DSP, General Purpose Signal Processing (GPSP) and application specific architecture for DSP.

DSP algorithm implementation demands using Application Specific Integrated Circuits (ASICs); costs for ASICs are high as well as algorithms should be verified and optimized before realization. The contemporary Field Programmable Gate Arrays (FPGAs) have emerged as a platform for efficient hardware implementation of such complex and computation intensive algorithms.
• High switching activity due to nature of test patterns
• Parallel activation of internal cores during test
• Power consumed by extra design-for-test(DFT) circuitry
• Low correlation among test vectors

This extra power consumption (average or peak) can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product yield and lifetime. Solutions that are commonly applied to alleviate the excessive power problem during test include reducing frequency and test partitioning/scheduling to avoid hot spots. The former disrupts at-speed test philosophy and the latter may significantly increase the time. Built-In Self-Test (BIST) is a DFT methodology that aims at detecting faulty components in a system by incorporating the test logic on chip. BIST is well known for its numerous advantages such as at-speed testing and reduced need for expensive external automatic test equipment (ATE). In BIST, a linear feedback shift register (LFSR) generates pseudorandom test patterns for primary inputs (for a combinational circuit) or scan chain inputs (for a sequential circuit). On the observation side, a multiple input signature register (MISR) compacts test responses received from primary outputs or scan chain outputs. Unfortunately, BIST-based structures are very vulnerable to high-power consumption during test. Test vectors, applied to a circuit under test at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The main reason is that the random nature of patterns generated by an LFSR significantly reduces the correlation not only among the patterns but also among adjacent bits within each pattern.

The rest of the paper is organized as follows. In section II, previous works relevant to power reduction are discussed, which mainly concentrated to reduce the average and peak power. In section III, an overview of power analysis for testing is presented. In section IV, Braun array multiplier is discussed briefly, which is taken here as a circuit under test (CUT) to verify the effectiveness of the proposed technique. In Section V, the proposed technique in the test pattern generator is discussed. Section VI describes the algorithm for the proposed LP-LFSR. In section VII, the implementation details and the results are presented. Section VIII summarizes the conclusion.

II. REVIEW OF PREVIOUS WORK

Different techniques are available to reduce the switching activities of test pattern, which reduce the power in test mode. For linear feedback shift register (LFSR), Giard proposed a modified clock scheme in which only half of the D flip-flops works, thus only half of the test pattern can be switched [7]. S.K. Guptha proposed a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. LT-TPG is proposed to reduce the average and peak power of a circuit during test [4]. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR).

Modifying the LFSR by adding weights to tune the pseudorandom vectors for various
probabilities decreases energy consumption and increases fault coverage [7], [8]. A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed in [9]. In this technique, an LFSR generates equally probable random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power. A better low power can be achieved by using single input change pattern generators. It is proposed that the combination of LFSR and scan shift register is used to generate random single input charge sequences [9 & 10]. In [10 &11], it is proposed that (2m-1) single input change test vectors can be inserted between two adjustment vectors generated by LFSR, m is length of LFSR. In [5], it is proposed that 2m single input changing data is inserted between two neighboring seeds. The average and peak power are reduced by using the above techniques. Still, the switching activities will be large when clock frequency is high.

### III. ANALYSIS OF POWER FOR TESTING

In CMOS technology, the power dissipation can be classified into static and dynamic. Static power dissipation is mainly due to the leakage current. Dynamic power dissipation is due to switching transient current and charging and discharging of load capacitances. Some significant parameters for evaluating the power consumption of CMOS circuits are discussed below.

\[ E_i = V_{dd}^2 C_0 F_i S_i \]  

Where \( V_{dd} \) is the supply voltage, \( C_0 \) is the load capacitance. The product of \( F_i \) and \( S_i \) is called weighted switching activity of internal circuit node i. The average power consumption of internal circuit I can be given by,

\[ P_i = V_{dd}^2 C_0 F_i S_i f \]  

\( f \) is the clock frequency. The summary of \( P_i \) of all the nodes is named as average power consumption. It can be observed from (1) and (2) that the energy and power consumption mainly depends on the switching activities, clock frequency and supply voltage. This paper reduces the switching activity at the inputs of the circuit under test (CUT) as low as possible.

#### A. BIST approach:

BIST is a design for testability (DFT) technique in which testing is carried out using built –in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in fig.1 needs three additional hardware blocks such as a pattern generator, a response analyzer and a test controller to a digital circuit. For pattern generators, we can use either a ROM with stored patterns, or a counter or a linear feedback shift register (LFSR). A response analyzer is a compactor with stored responses or an LFSR used as a signature analyzer. A controller provides a control signal to activate all the blocks. BIST has some major drawbacks where architecture is based on the linear feedback shift register (LFSR). The circuit introduces more switching activities in the circuit under test (CUT) during test than that during normal operation[5]. It causes excessive power
dissipation and results in delay penalty into the design[6].

B. Classification of test strategies:

1. Weighted Pseudorandom: Testing: In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudorandom testing. Thus, the test length can be effectively shortened.

2. Pseudo exhaustive Testing: Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flaws within the sub circuits can be detected. However, such a method involves extra design effort to partition the circuits and deliver the test patterns and test responses. BIST is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. BIST is the commonly used design technique for self testing of circuits.

3. Pseudorandom Testing: Pseudorandom testing involves the application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order. The test length and the contents of the patterns are used to impart fault coverage.

4. Exhaustive Testing: Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT). It guarantees that all detectable faults that divert from the sequential behavior will be detected. The strategies are often applied to complex and well isolated small modules such as PLAs.

5. Stored Patterns: Stored-pattern approach tracks the pre generated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self test of a computer and microprocessor functional testing using micro programs.

IV. DESIGN OF MULTIPLIER

Braun’s multiplier is an n×m bit parallel multiplier and generally known as carry save multiplier and is constructed with m×(n-1) addresses and m×n AND gates. The Braun’s multiplier has a glitching problem which is due to the ripple carry adder in the last stage of the multiplier.

The simplest way to perform a multiplication is to use a single two input adder. For inputs that are M and N bits wide, the multiplication tasks M cycles, using an N-bit adder. This shift–and–add algorithm for multiplication adds together M partial products. Each partial product is generated by multiplying the multiplicand with a bit of the multiplier –which, essentially, is an AND operation –and by shifting the result in the basis of the multiplier bit’s position. Similar to the familiar long hand decimal multiplication, binary multiplication involves the addition of shifted versions of the multiplicand based on the value and position of each of the multiplier bits. As a matter of fact, it’s much simpler to perform binary multiplication than decimal multiplication. The value of each digit of a binary number can only be 0 or 1, thus, depending on the value of the multiplier bit, the partial products can only be a copy of the multiplicand, or 0.
V. PROPOSED METHOD

Because of simplicity of the circuit and less area occupation, linear feedback shift register [LFSR] is used at the maximum for generating test patterns. In this paper, we proposed a novel architecture which generates the test patterns with reduced switching activities. LP-TPG structure consists of modified low power linear feedback shift register (LPLFSR), m-bit counter, gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2^m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated from LP-LFSR is Exclusive–ORed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.

VI. ALGORITHM FOR LP-LFSR

The algorithm for LP-LFSR is given below:

- Consider a N-bit external (or) internal linear feedback shift register [n>2].
- For example n-bit, external LFSR is taken, which consists of n-flip flops in series. A common clock signal is applied as control signal for all flip flop.
- For exchanging the output of adjacent flip flops, multiplexers are used. The output of the last stage flip flop is taken as a select line.
- If the last stage flip flop output is one, any one of the flip flop output is swapped with its adjacent flip flop output value.
- If the last stage flip flop output is Zero, no swapping will be carried out.
- The output from other flip flops will be taken as such.
- If the LFSR is moved through a complete cycle of 2n states then the transitions expected are 2n-1. When the output of the adjacent flip flops are swapped, the expected transitions are 2n-2. Thus the transitions produced are reduced by 50% compared with original LFSR.
transition reduction is concentrated mainly on any one of the multiplexer output.

- Gray converter modifies the counter output such that two successive values of its output are differing in only one bit. Gray converters can be implemented as shown below.

\[ g[n-1] = k[n-1] \]
\[ g[n-2] = k[n-1] \oplus k[n-2] \]
\[ \ldots \]
\[ g[1] = k[1] \oplus k[2] \]
\[ g[0] = k[0] \oplus k[1] \]

In [12] it is stated that that the conventional LFSR’s outputs cannot be taken as the seed directly, because some seeds may share the same vectors. Thus the LP-LFSR should ensure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. Test patterns generated from the proposed structure are implemented as following equations.

\[ x[0] = f[0] \oplus g[0] \]
\[ x[1] = f[1] \oplus g[1] \]
\[ \ldots \]
\[ X[n-1] = f[n-1] \oplus g[n-1] \]

Thus the XOR result of the sequences is single input changing sequence. In turn reduces the switching activity and so power dissipation is very less compared with conventional LFSR. Fig. 3 is an example of counter and its respective gray value. It is shown that all values of \( g[2:0] \) are single input changing patterns.

### IV. IMPLEMENTATION AND RESULTS

The proposed low power linear feedback shift register [LP-LFSR] designed using Verilog hardware description language and structural form of coding. The proposed system simulation results are as follows:

- Patterns:
  - \( K[2:0] g[2:0] \)
  - \( K0=000 \quad g0=000 \)
  - \( K1=001 \quad g1=001 \)
  - \( K2=010 \quad g2=011 \)
  - \( K3=011 \quad g3=010 \)
  - \( K4=100 \quad g4=110 \)
  - \( K5=101 \quad g5=111 \)
  - \( K6=110 \quad g6=101 \)
  - \( K7=111 \quad g7=100 \)
VIII. CONCLUSION

A low power test pattern generator has been proposed which consists of a modified low power linear feedback shift register (LP-LFSR). The seed generated from (LP-LFSR) is EX-ORed with the single input changing sequences generated from gray code generator, which effectively reduces the switching activities among the test patterns. Thus the proposed method significantly reduces the power consumption during testing mode with minimum number of switching activities using LP-LFSR in place of conventional LFSR in the circuit used for test pattern generator. From the implementation results, it is verified that the proposed method gives better power reduction compared to the exiting method.

VII. REFERENCES


AUTHORS

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